

FIG. 6-1 V COUNTER

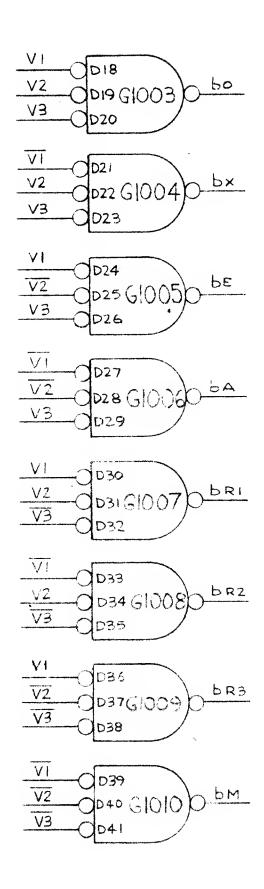


FIG 6-2 V COUNT DECODER

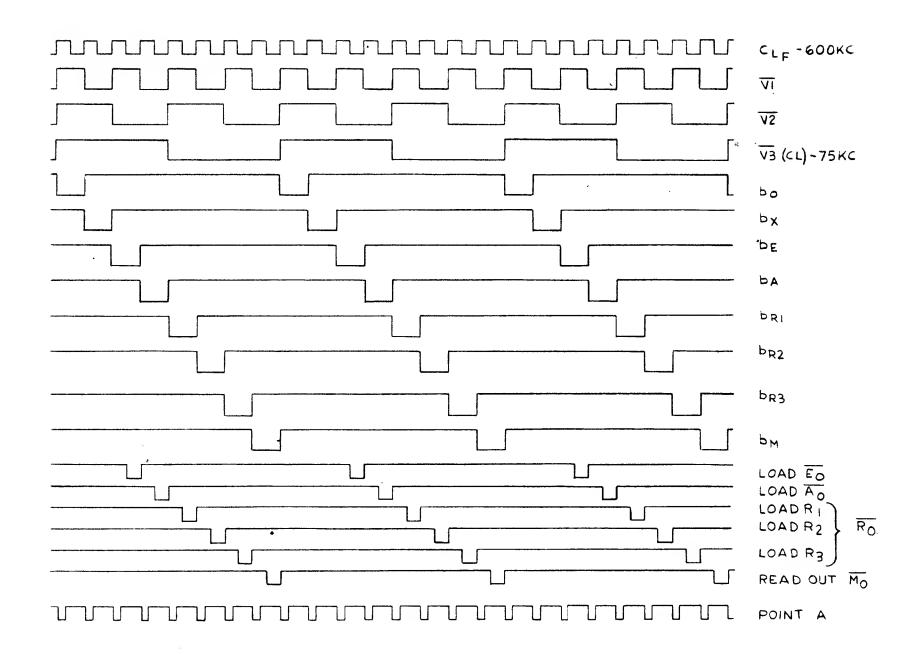


FIG. 6-3 SUB-BIT TIMING

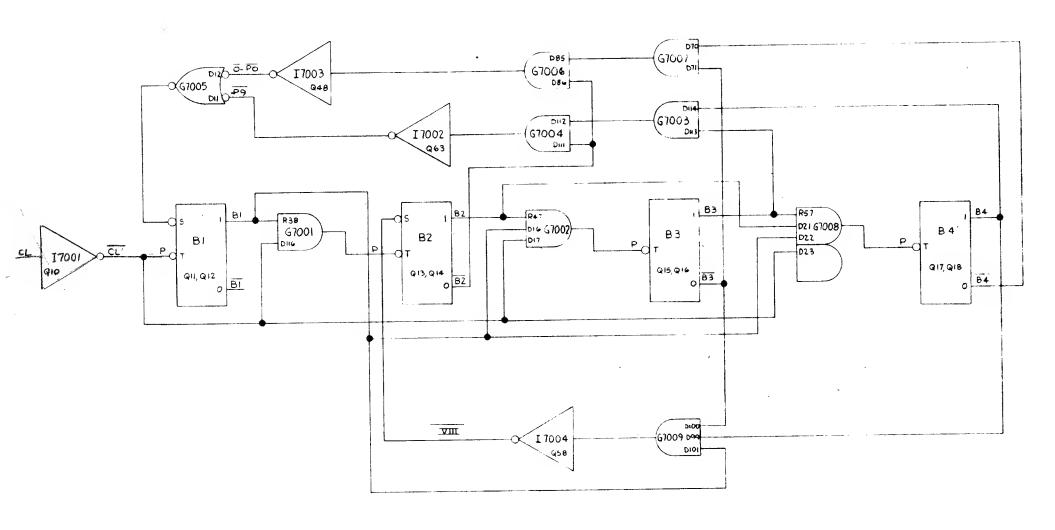


FIG. 6-4
BIT COUNTER

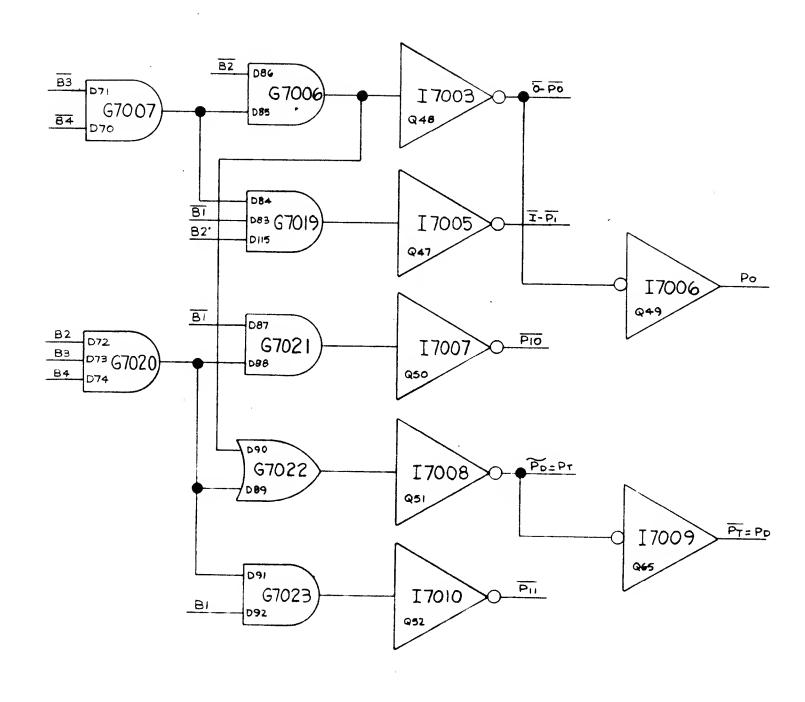


FIG. 6-5 BIT COUNT DECODER (SHT. 10F2)

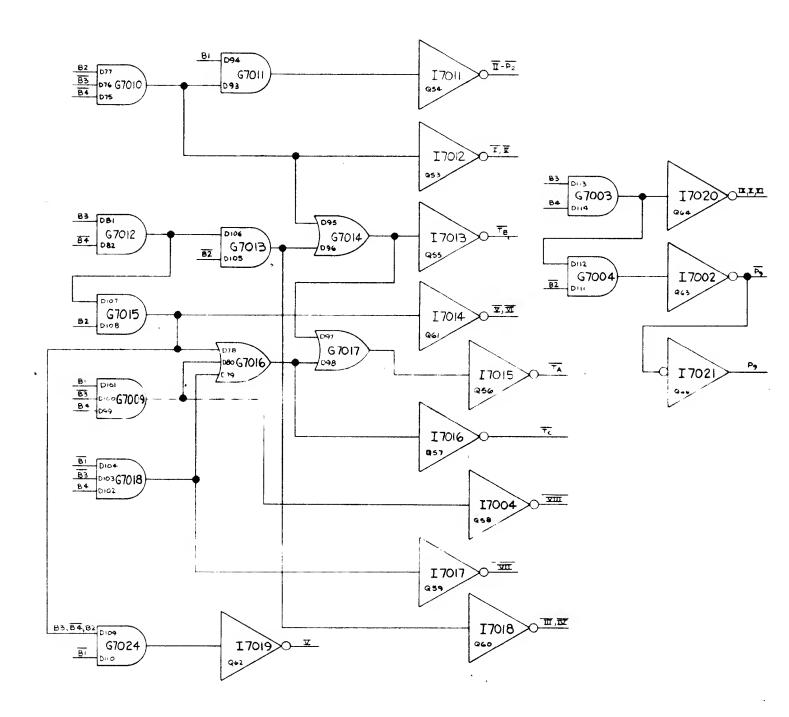


FIG. 6-5 BIT COUNT DECODER

(SHT 2 OF 2)

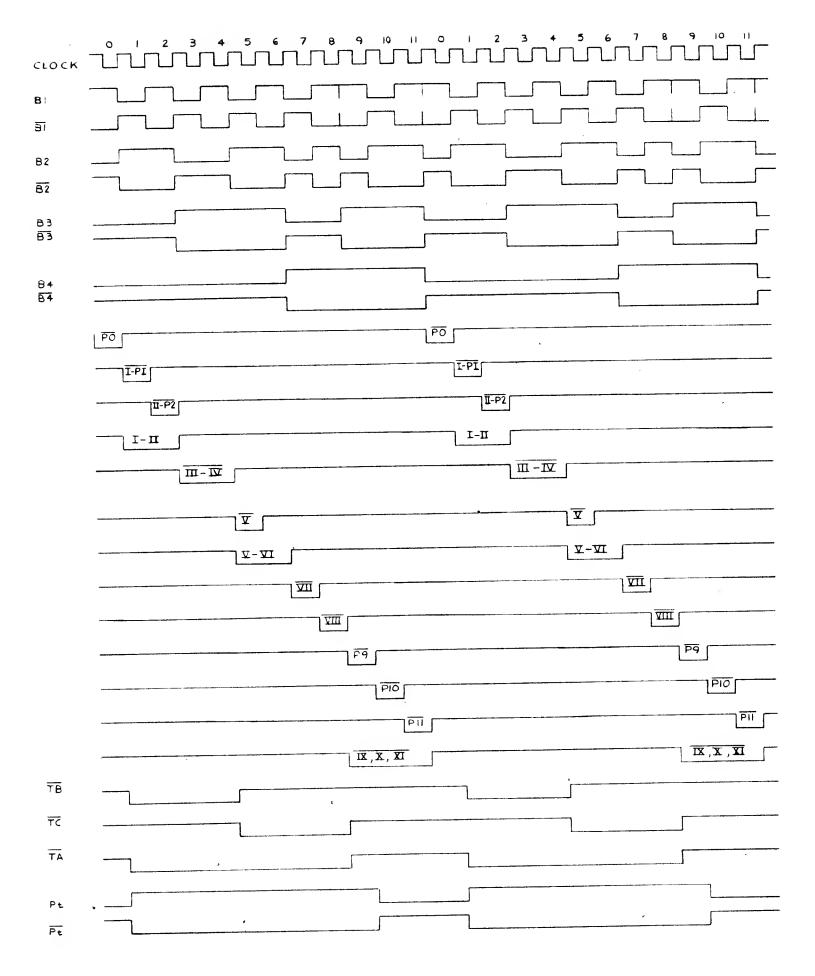


FIG. 6-6 BIT TIMING

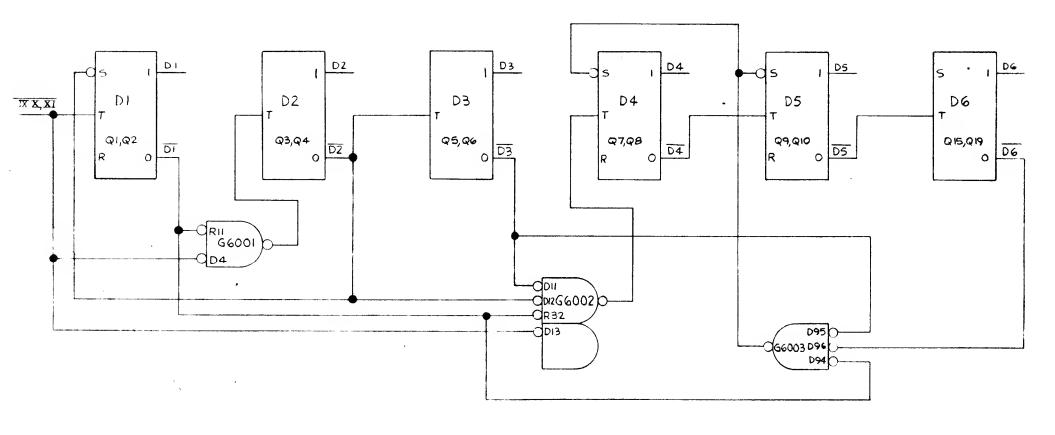


FIG. 6-7 DIGIT COUNTER

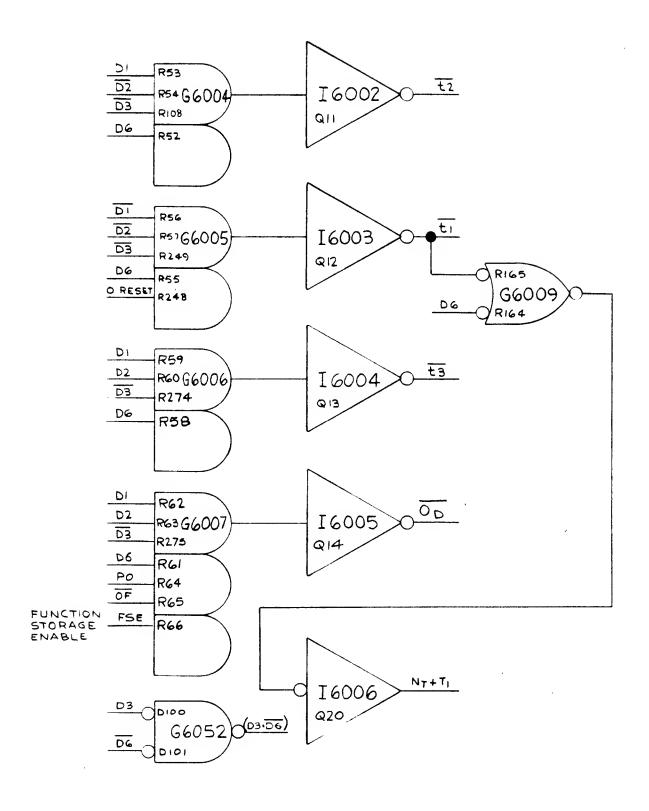


FIG. 6-8
DIGIT COUNT DECODER

(SHEET 1 OF 2)

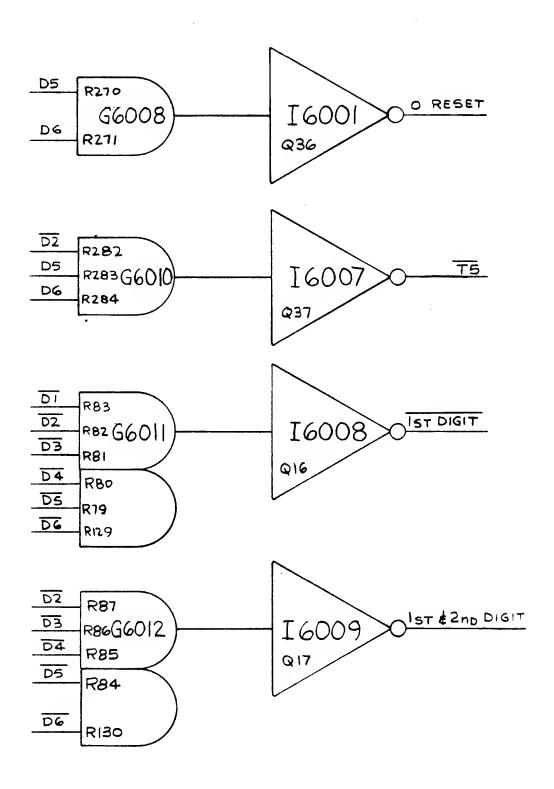


FIG. 6-8 DIGIT COUNT DECODER

(SHEET 2 0 F 2)

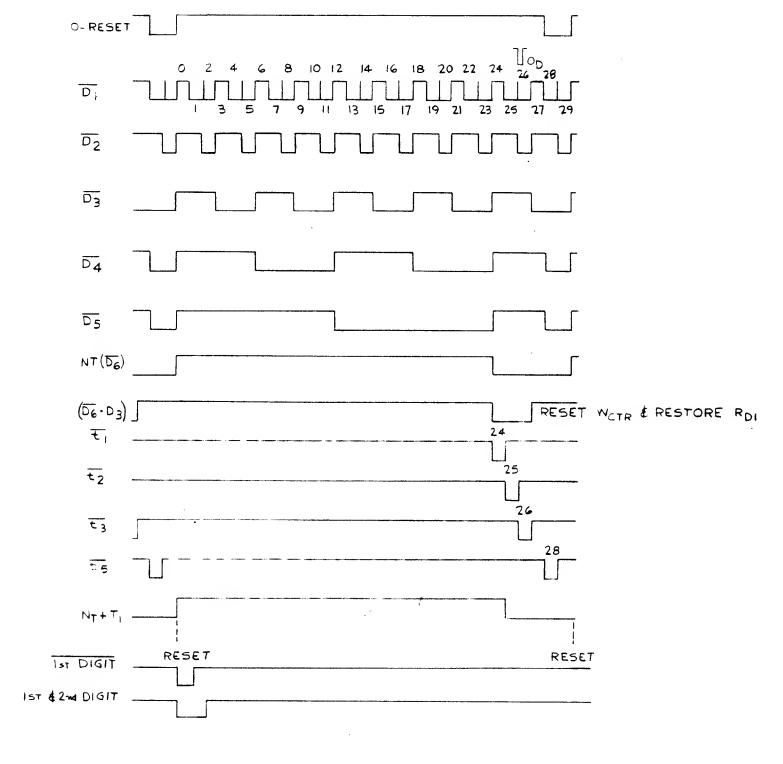


FIG. 6-9 DIGIT TIMING

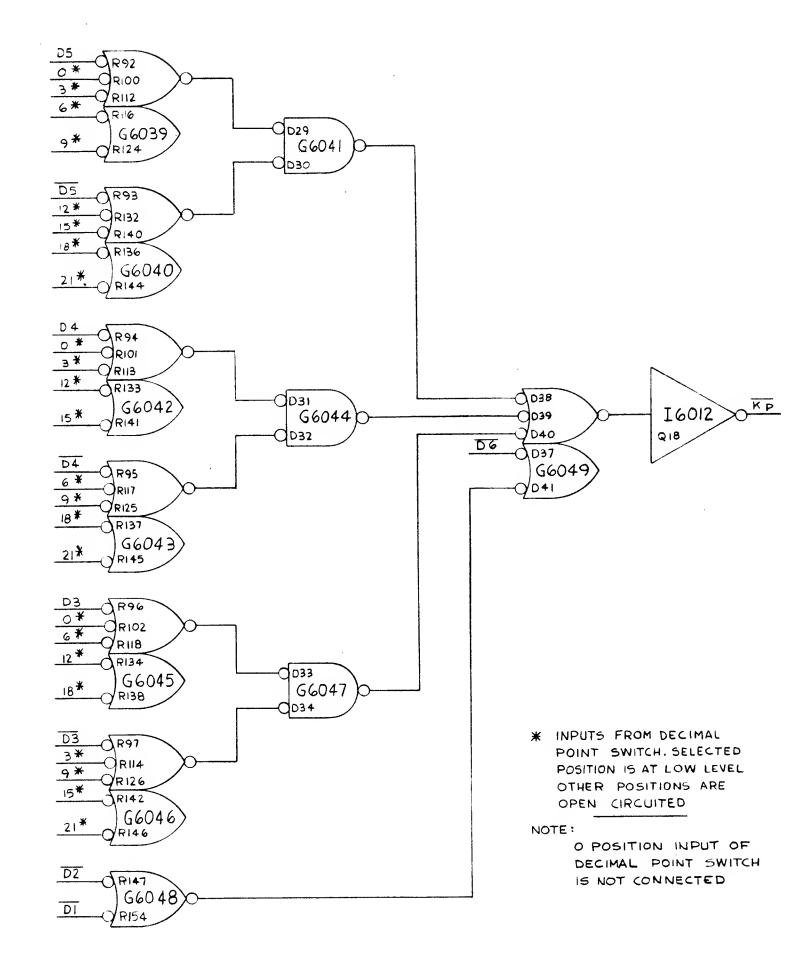


FIG. 6-10 Kp LOGIC

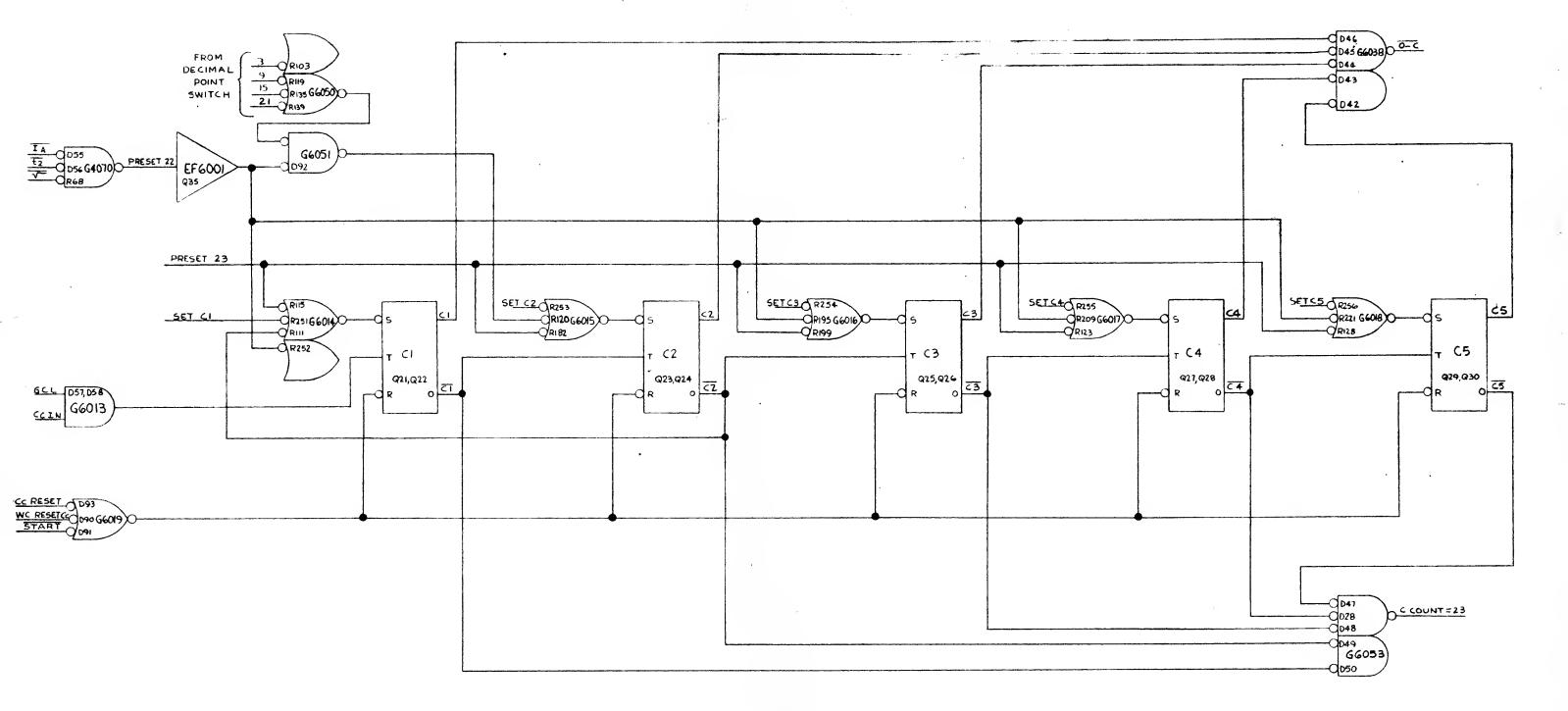


FIG G-II

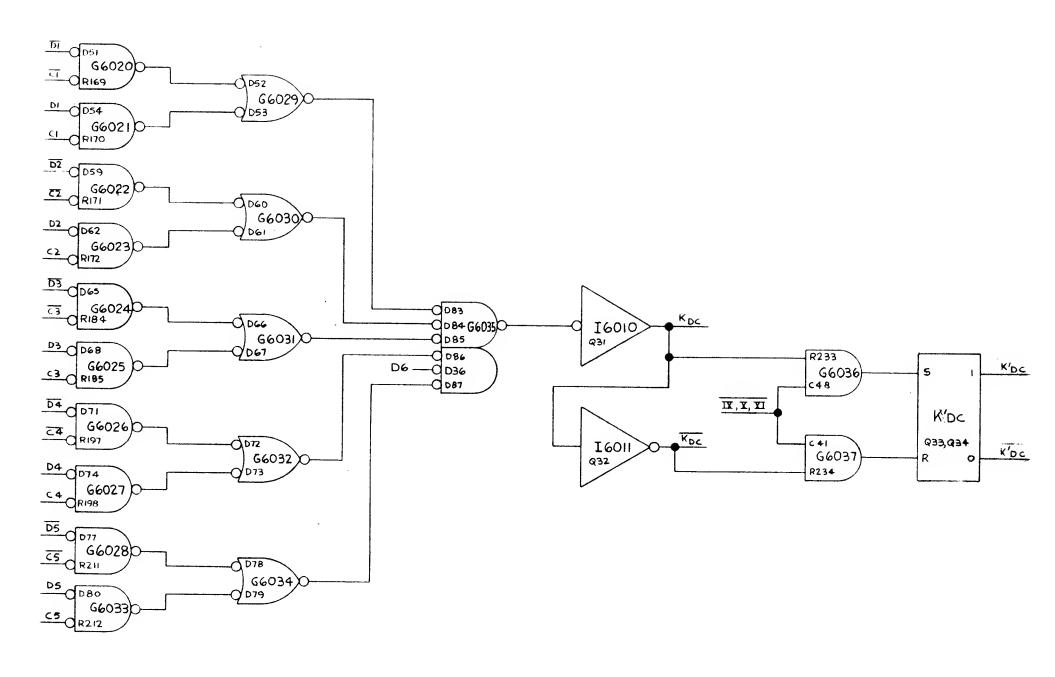


FIG. 6-12 K DC' K'DC LOGIC

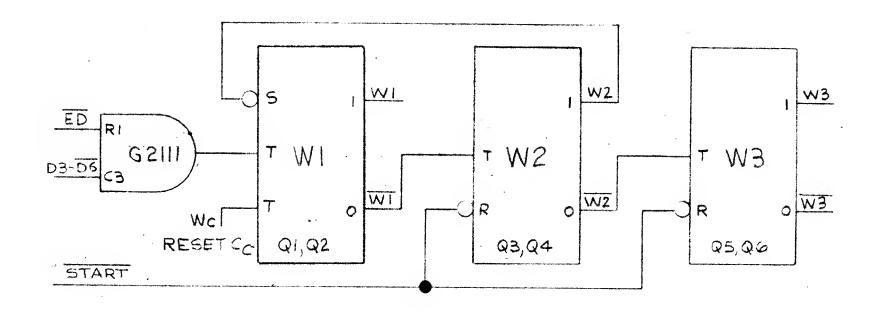


FIG. 6-13 WORD COUNTER

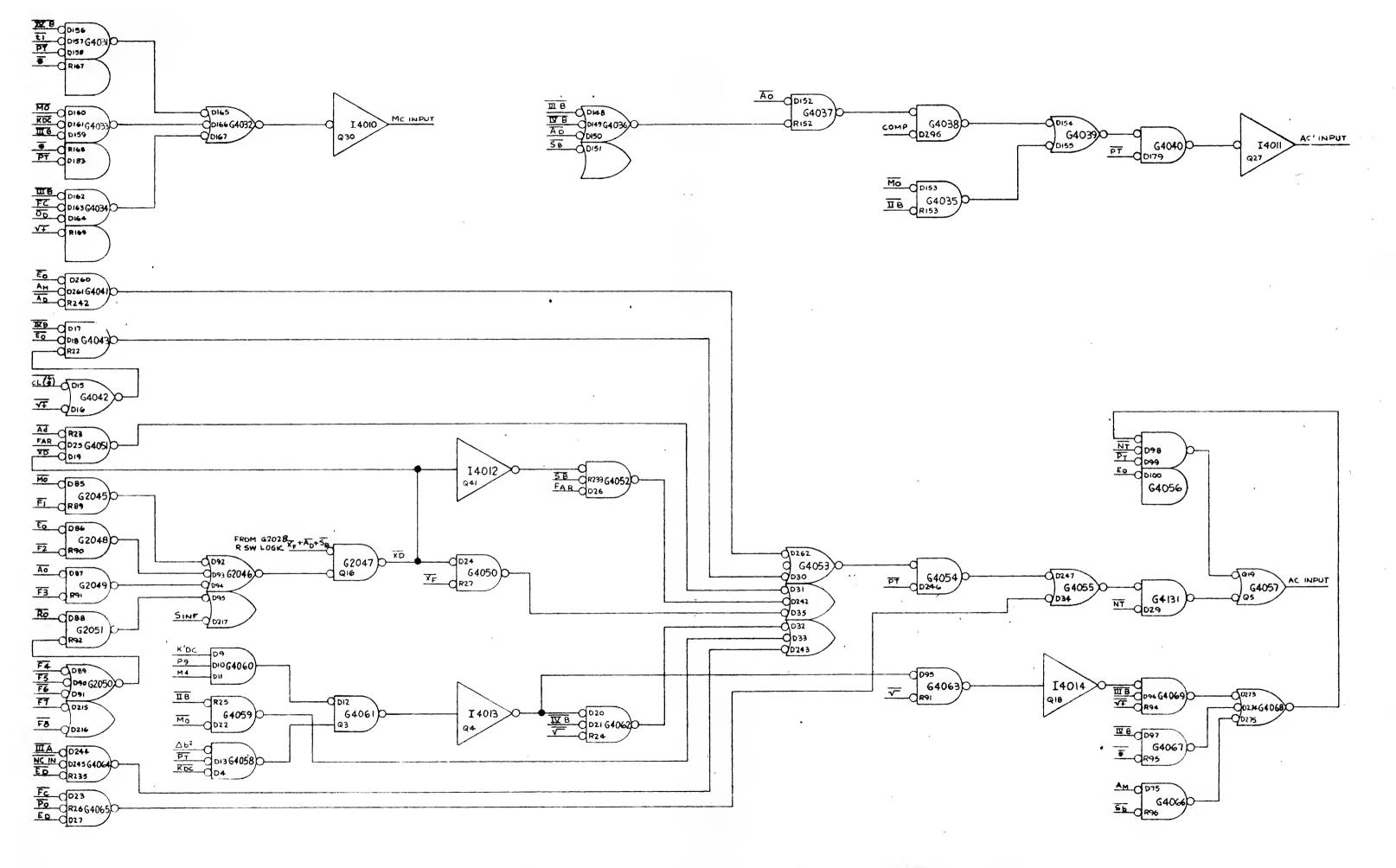


FIG. 6-14: A COUNTER AND M COUNTER AC IN, AC' IN AND MC IN GATES

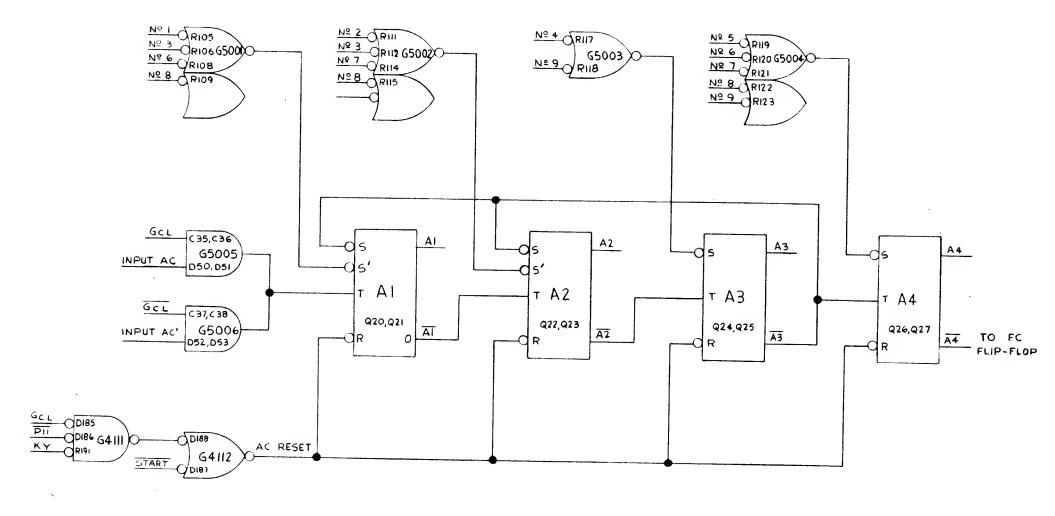


FIG. 6-15 A COUNTER

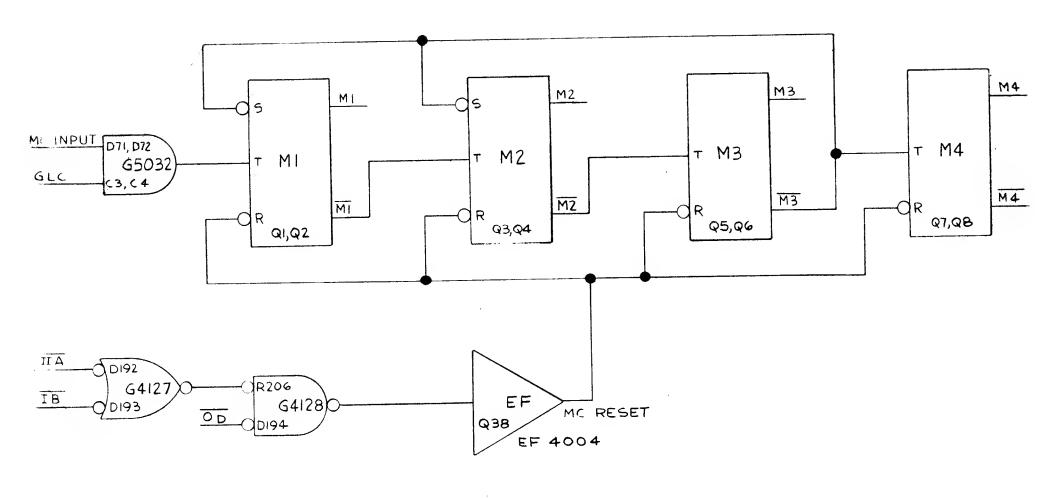


FIG. 6-16 M COUNTER

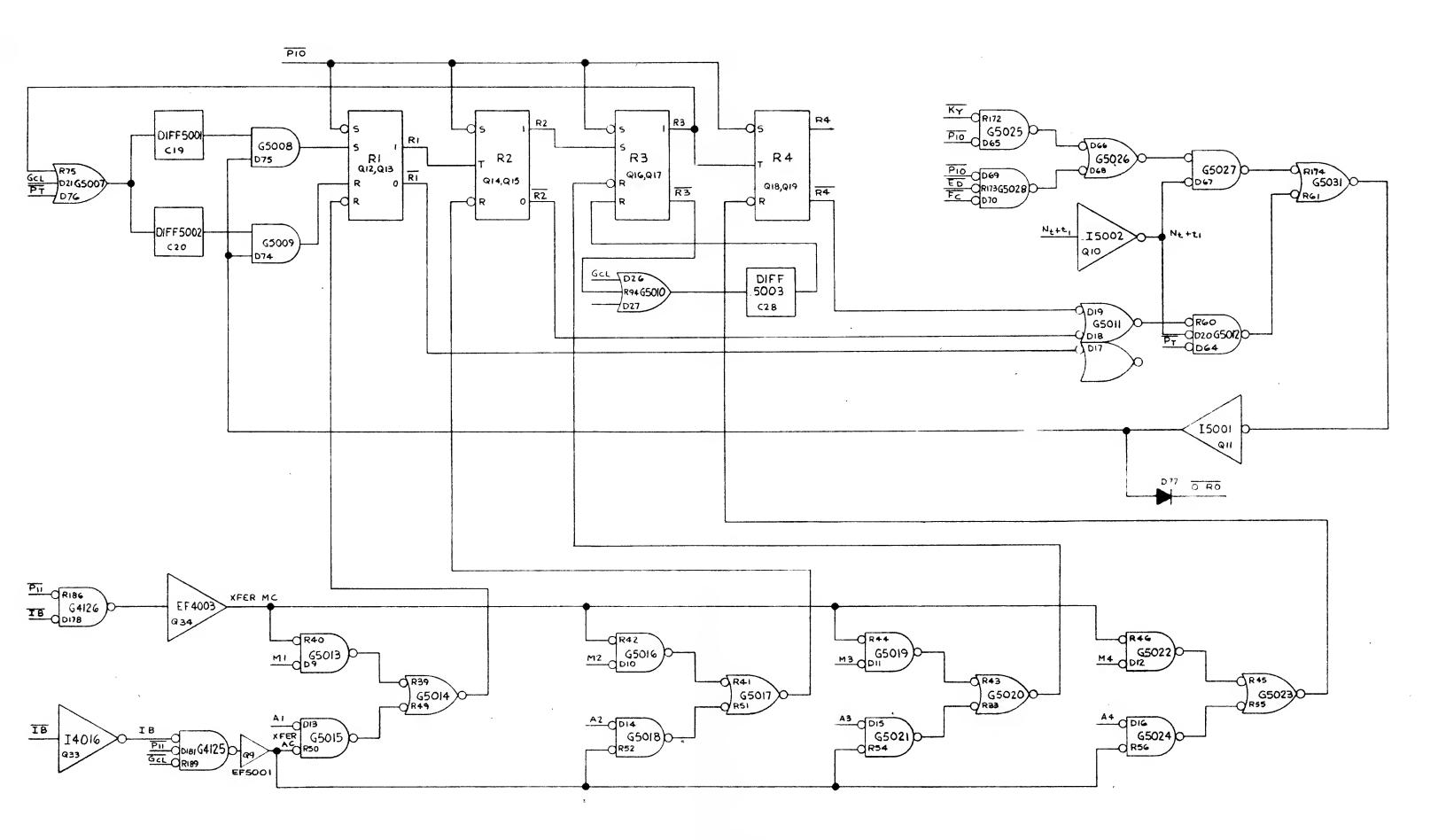


FIG G-17 R COUNTER

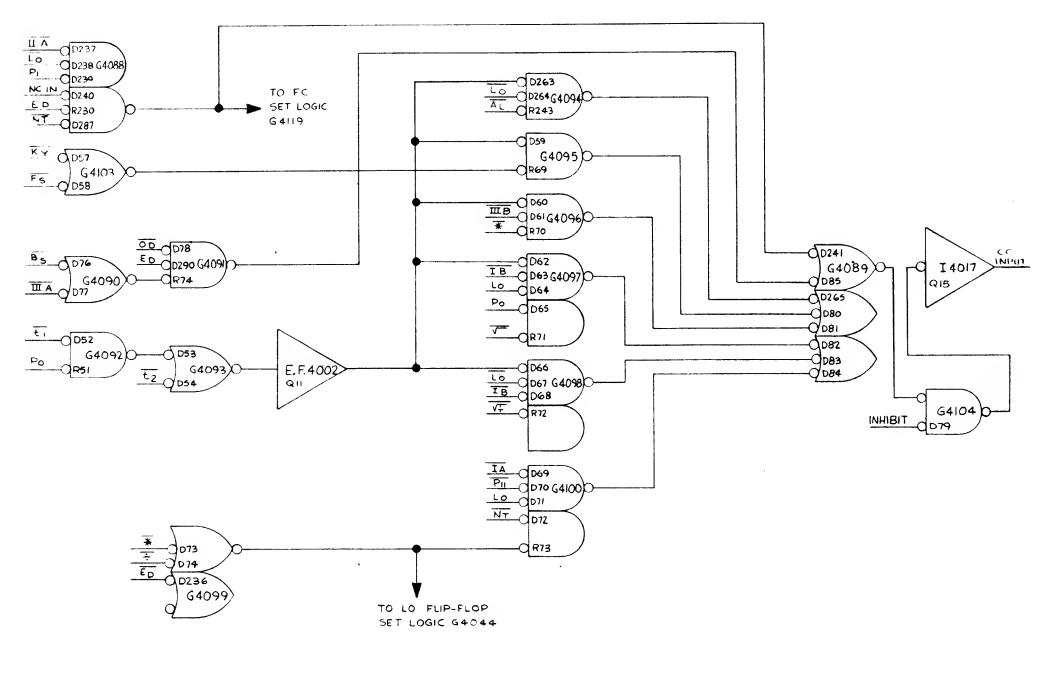
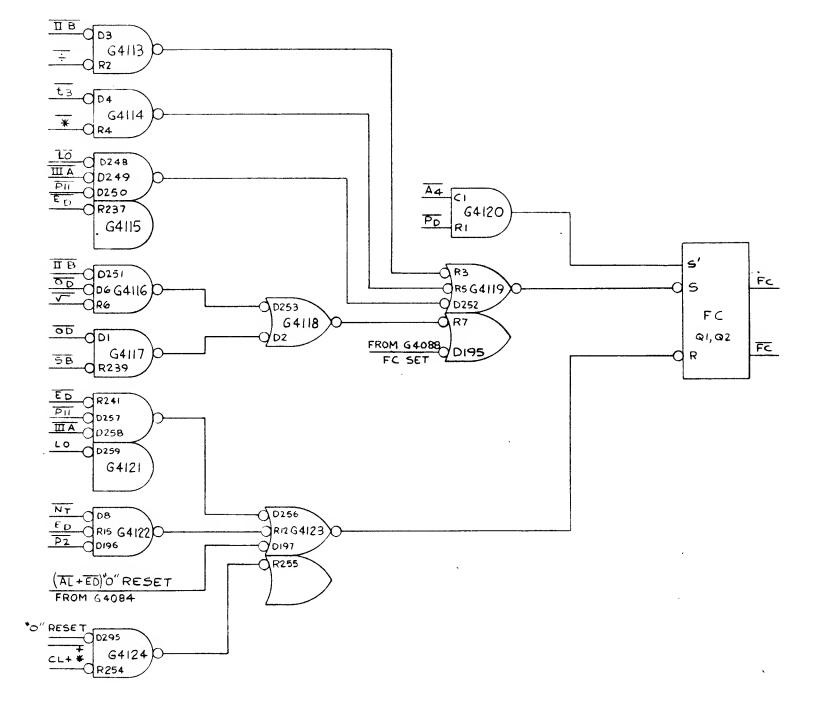


FIG.6-18: C COUNTER INPUT GATES



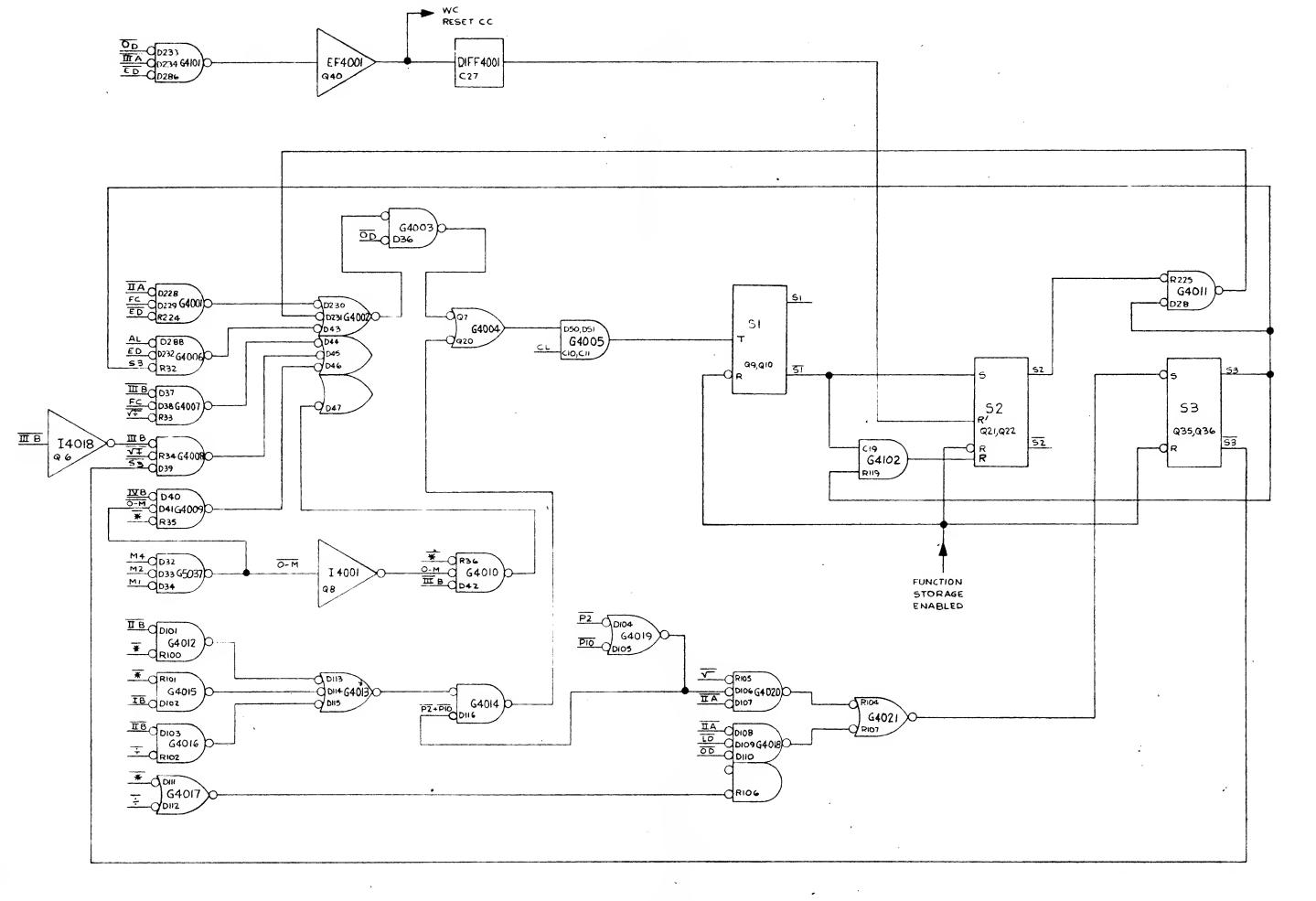


FIG. 6-20 CYCLE COUNTER

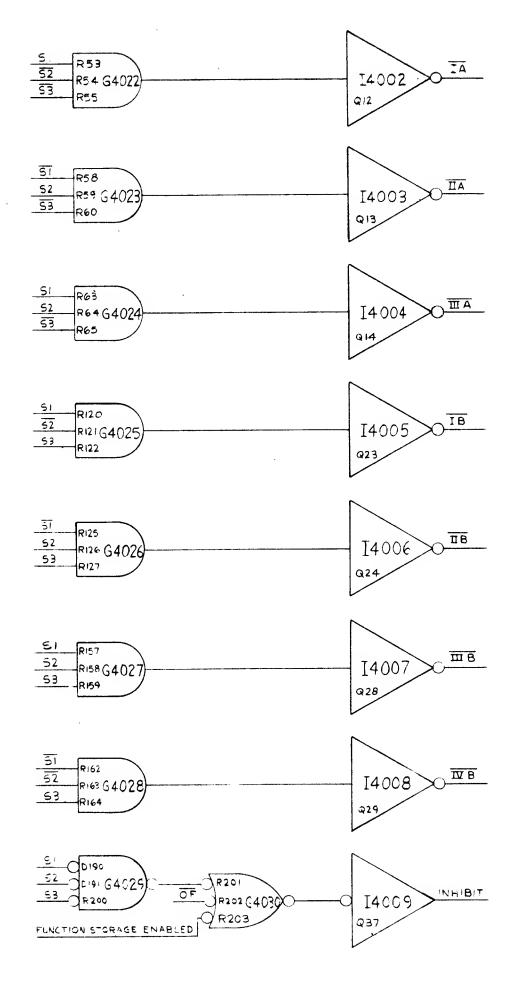


FIG. 6-21: CYCLE COUNT DECODER
AND INHIBIT LOGIC

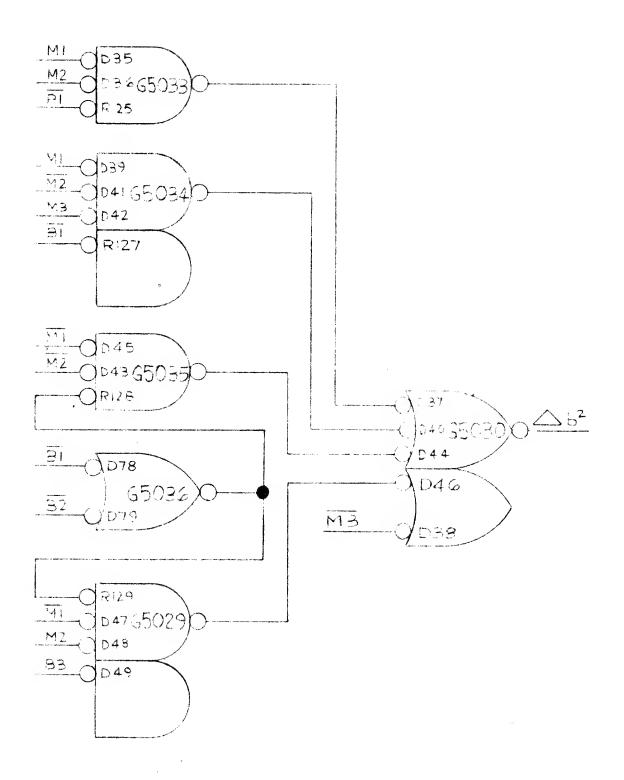
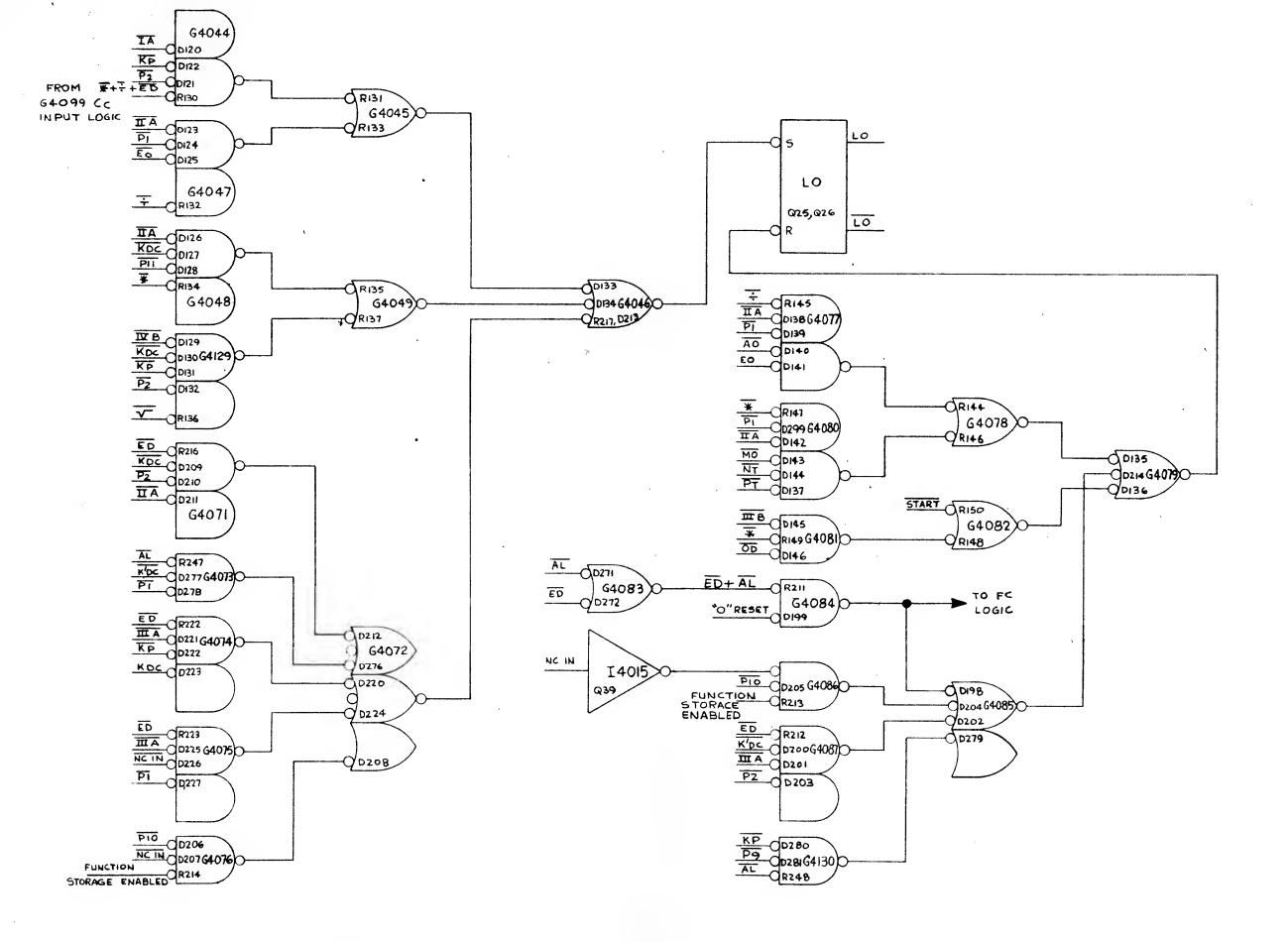


FIG. 6-22: △B2 GENERATOR



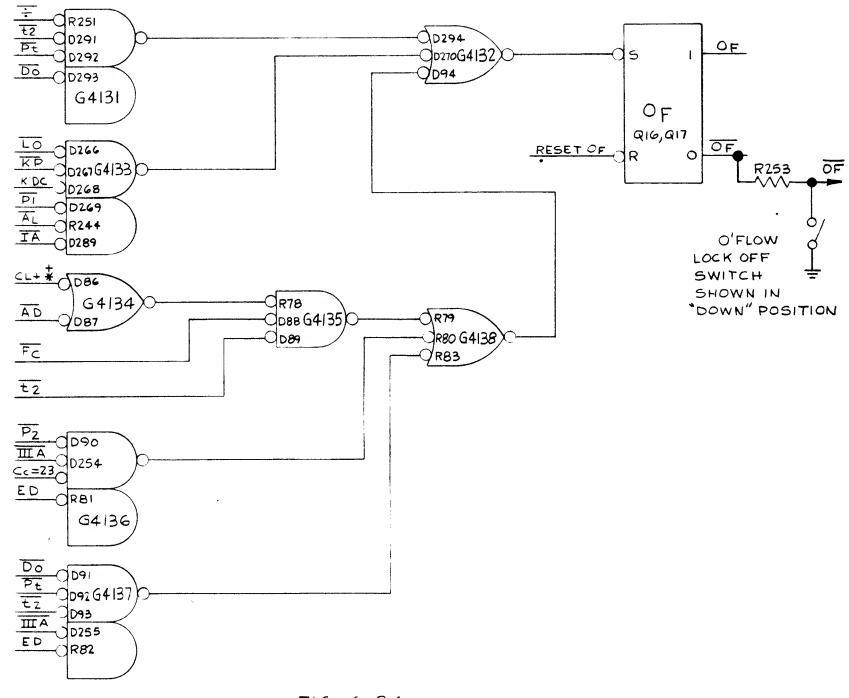


FIG. 6-24 OF LOGIC

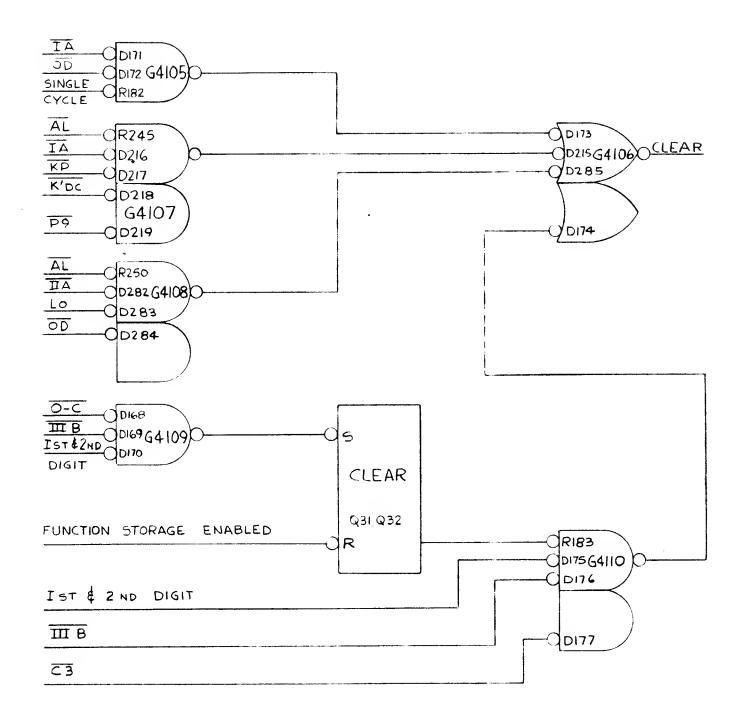


FIG. 6-25: CLEAR LOGIC

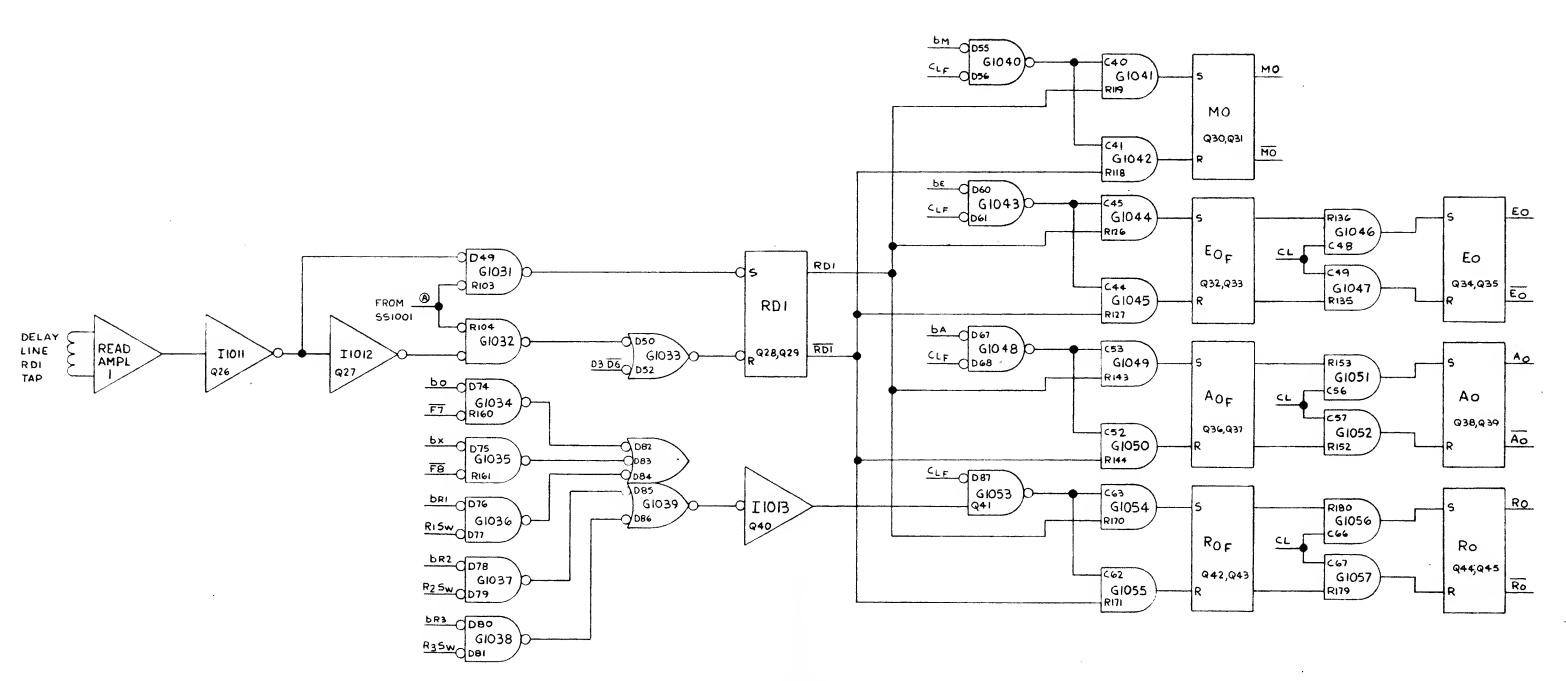


FIG 6-26 DEMULTIPLE XER LOGIC

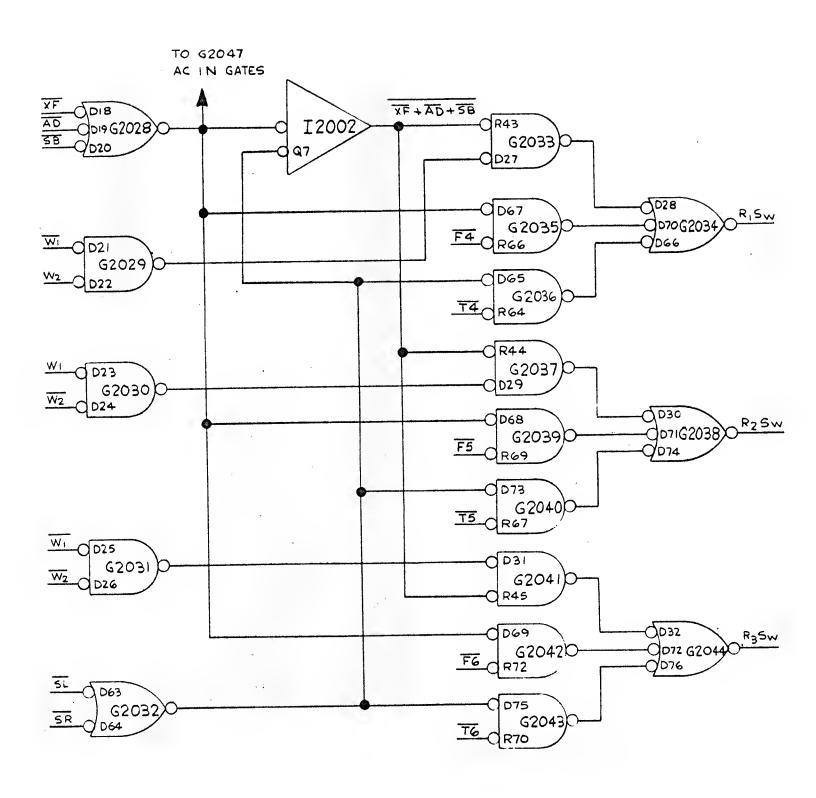


FIG. 6-27: R SW LOGIC

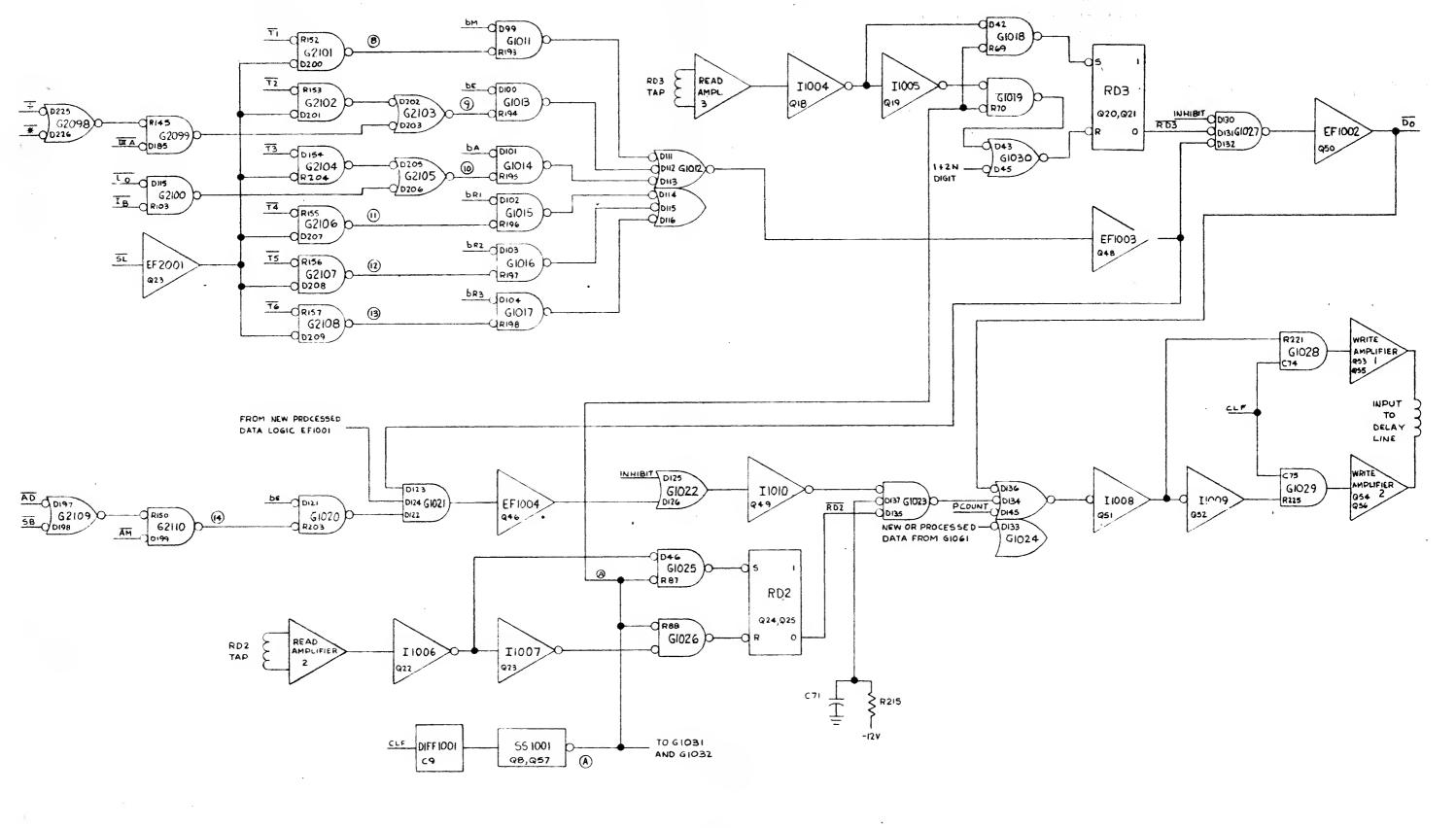


FIG. 6-28 SHIFT LEFT, RECIRCULATE LOGIC

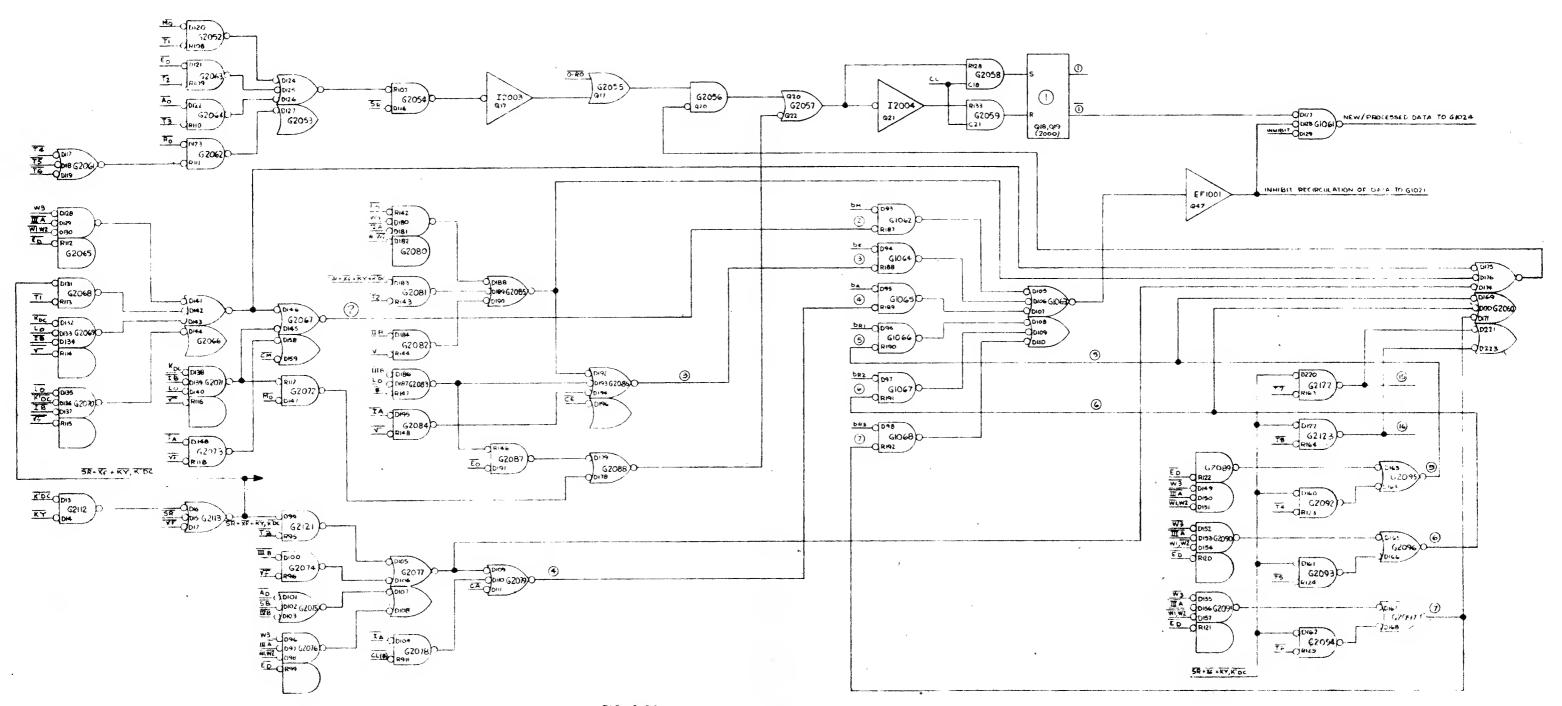


FIG. 6-29

RECORD NEW/PROCESSED DATA,
SHIFT RIGHT, EPASE LOGIC

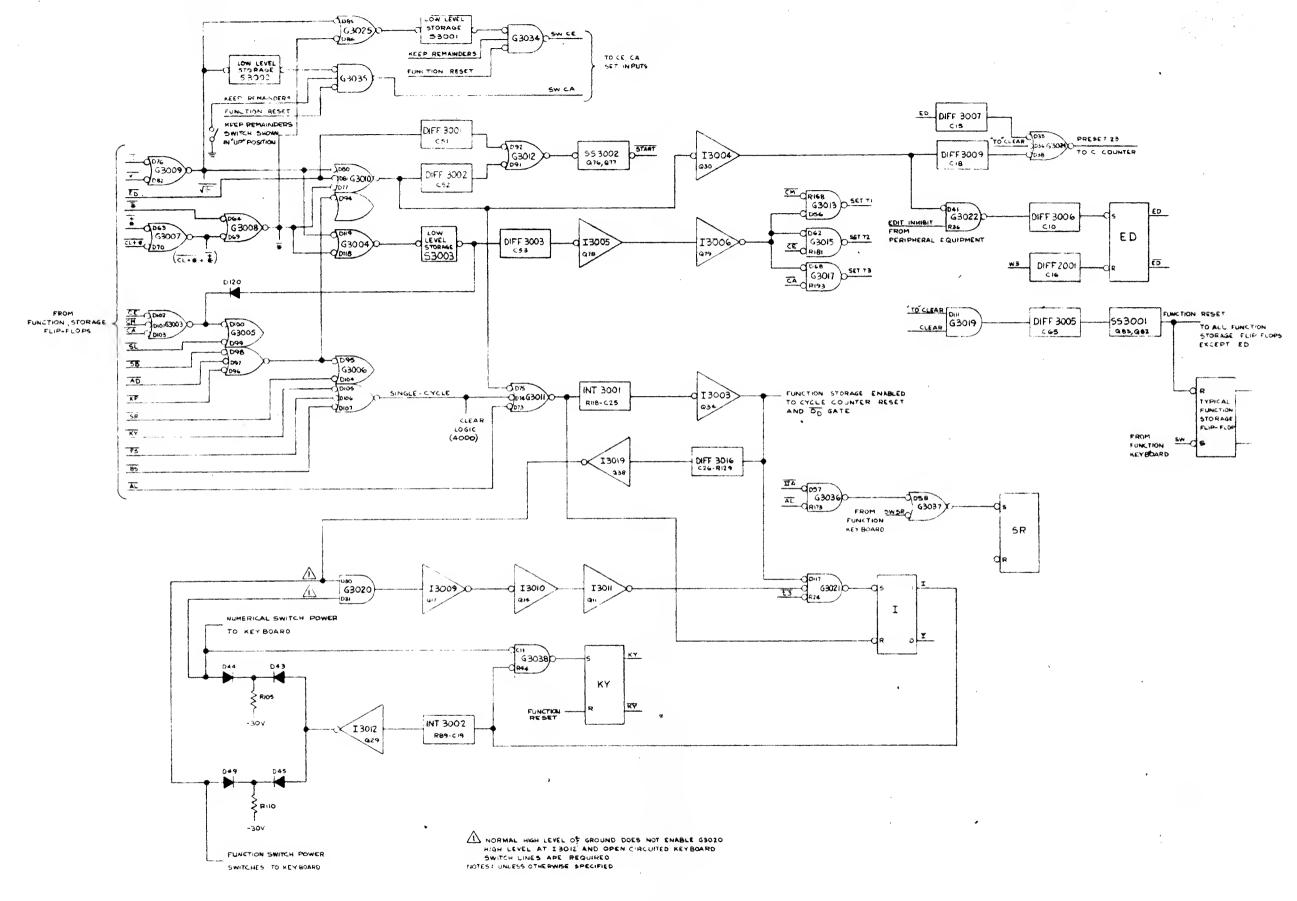
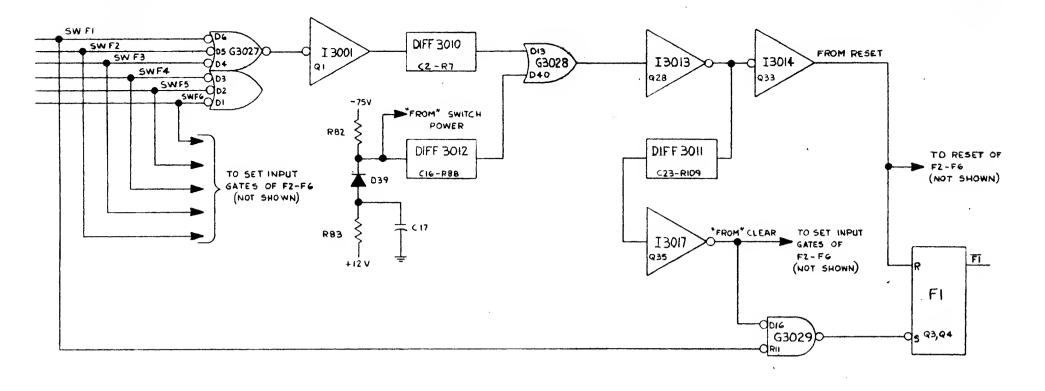


FIG. 6-30 FUNCTION CONTROL LOGIC



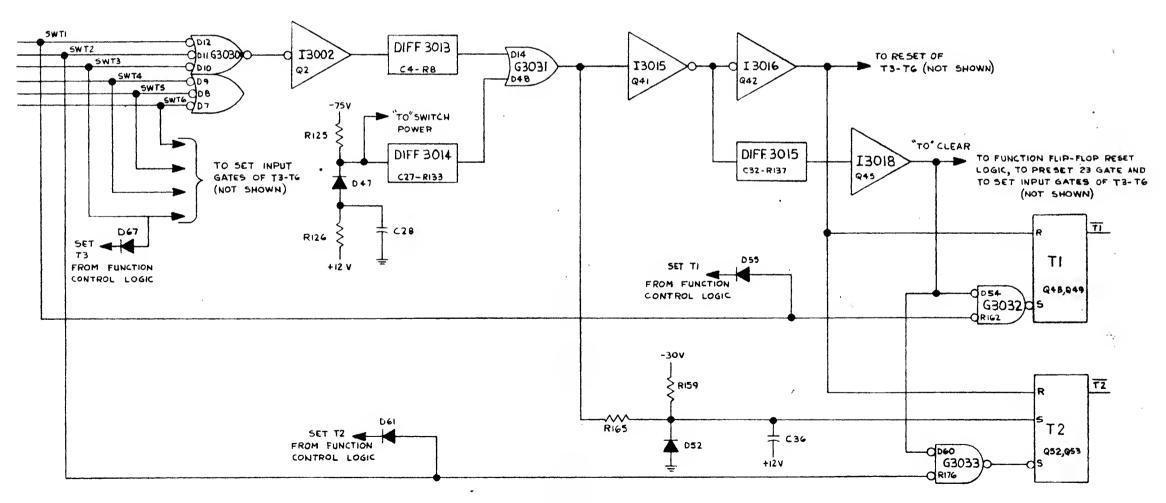


FIG. 6-31 . "TO" FROM" STORAGE AND CONTROL LOGIC

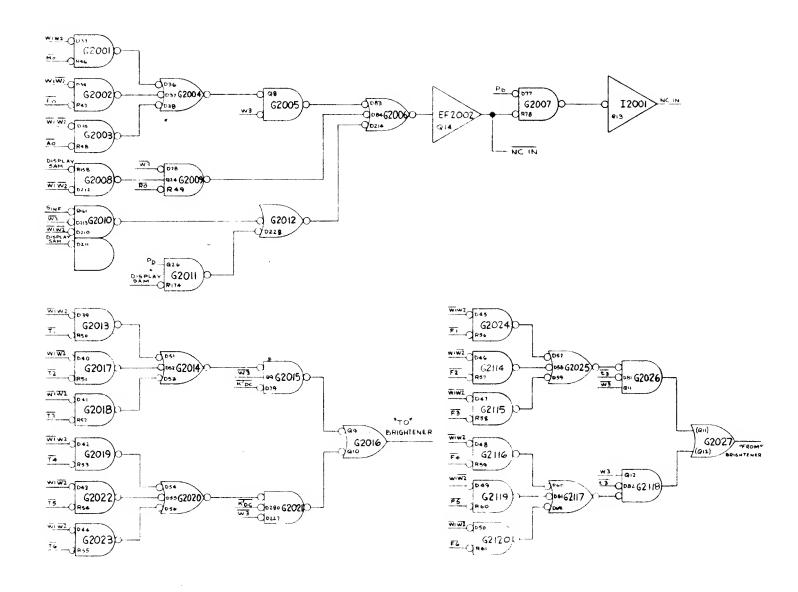
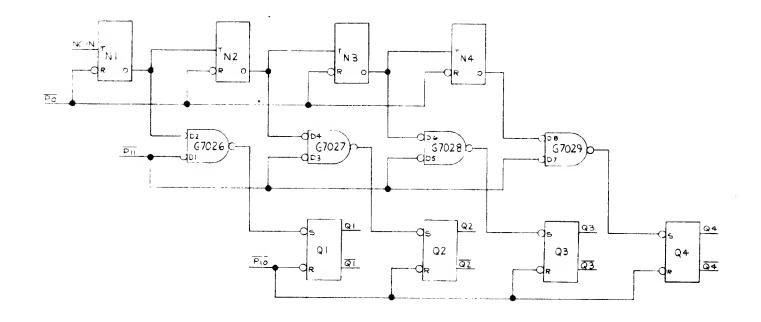


FIG. 6-32: NC INPUT, "TO" BRIGHTENER, FROM" BRIGHTENER LOGIC



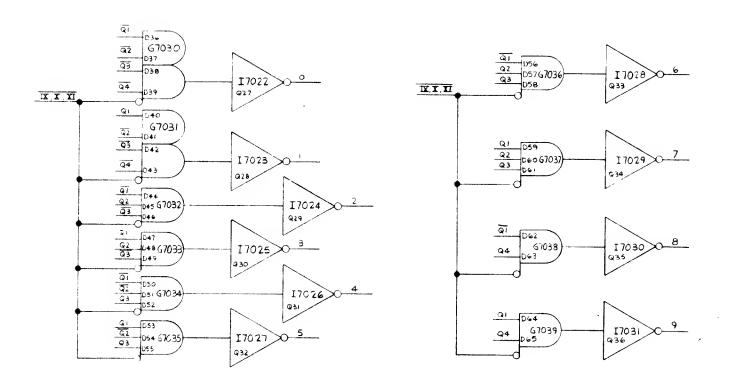


FIG. 6-33: CHARACTER (N) COUNTER, STORAGE (Q) REGISTER, AND DE CODER LOGIC

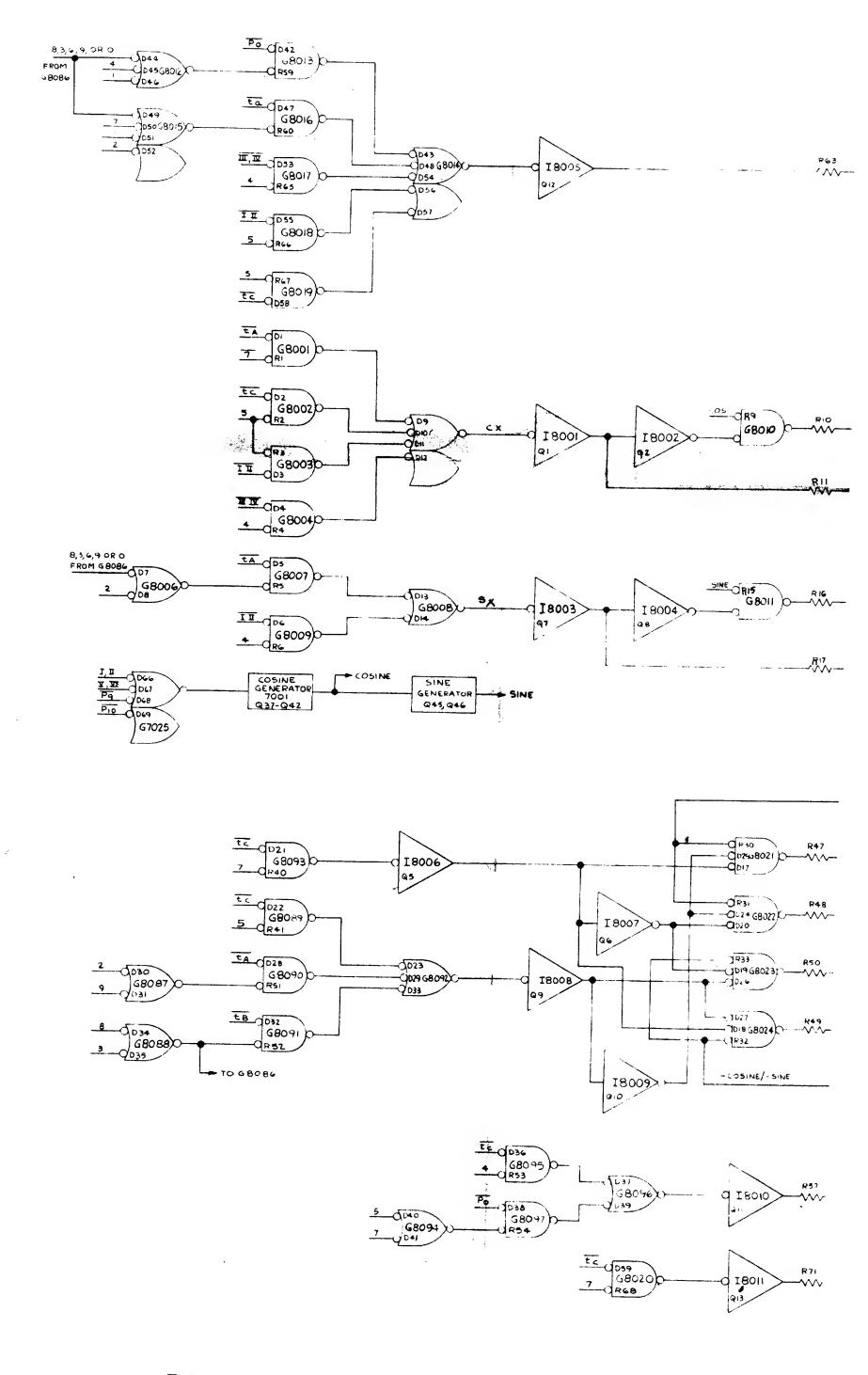


FIG 6-34 OPTICAL CODER

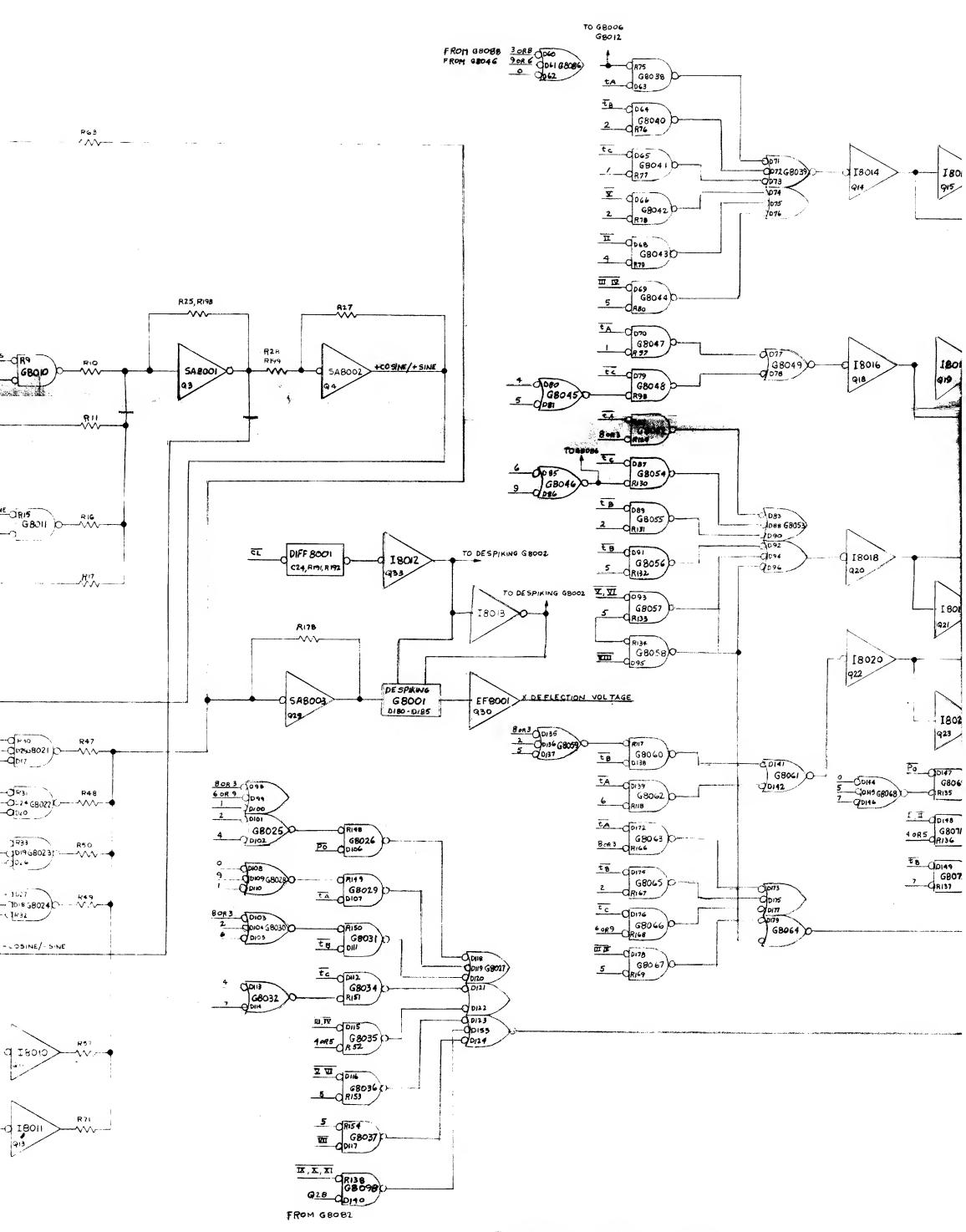
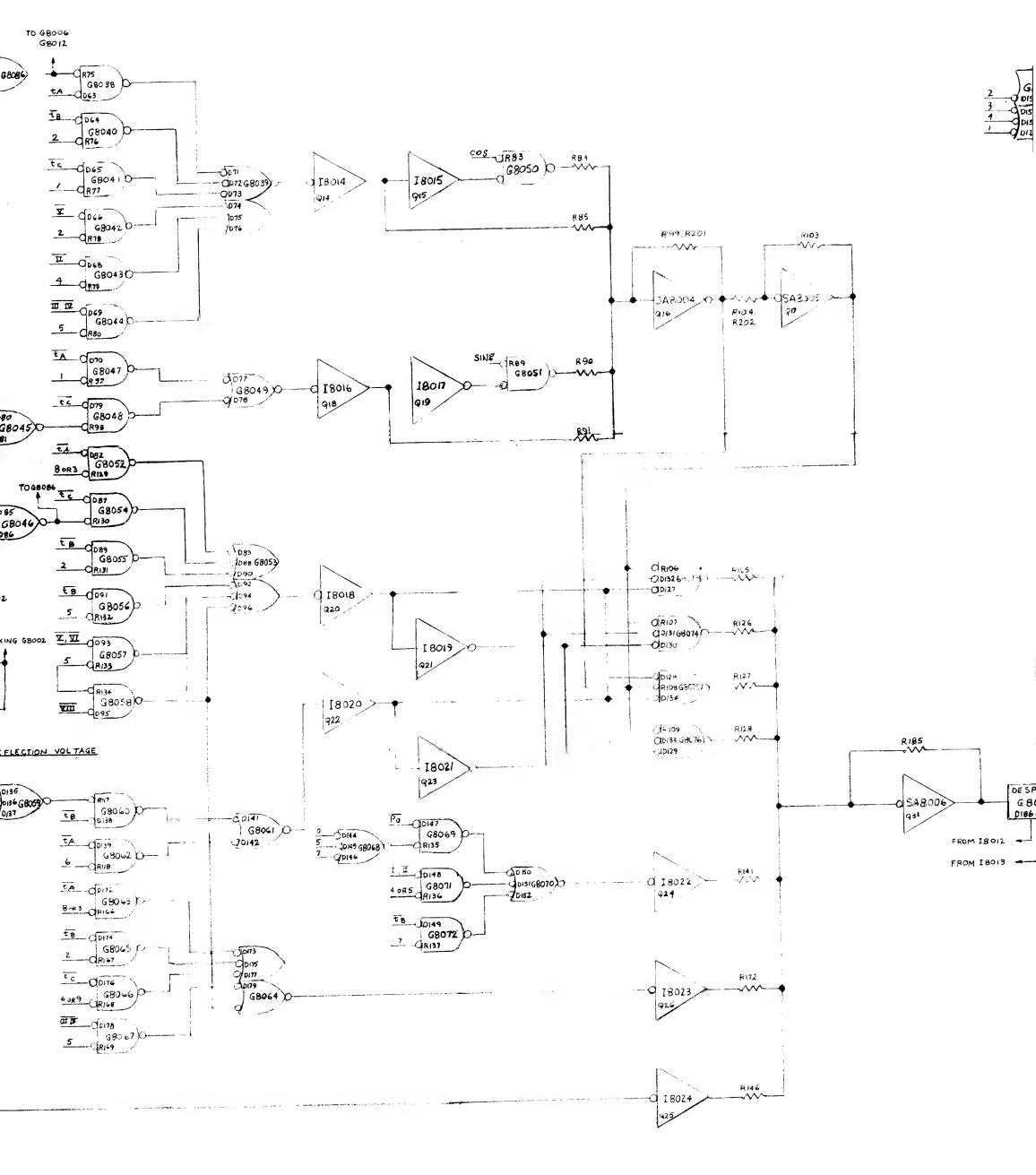
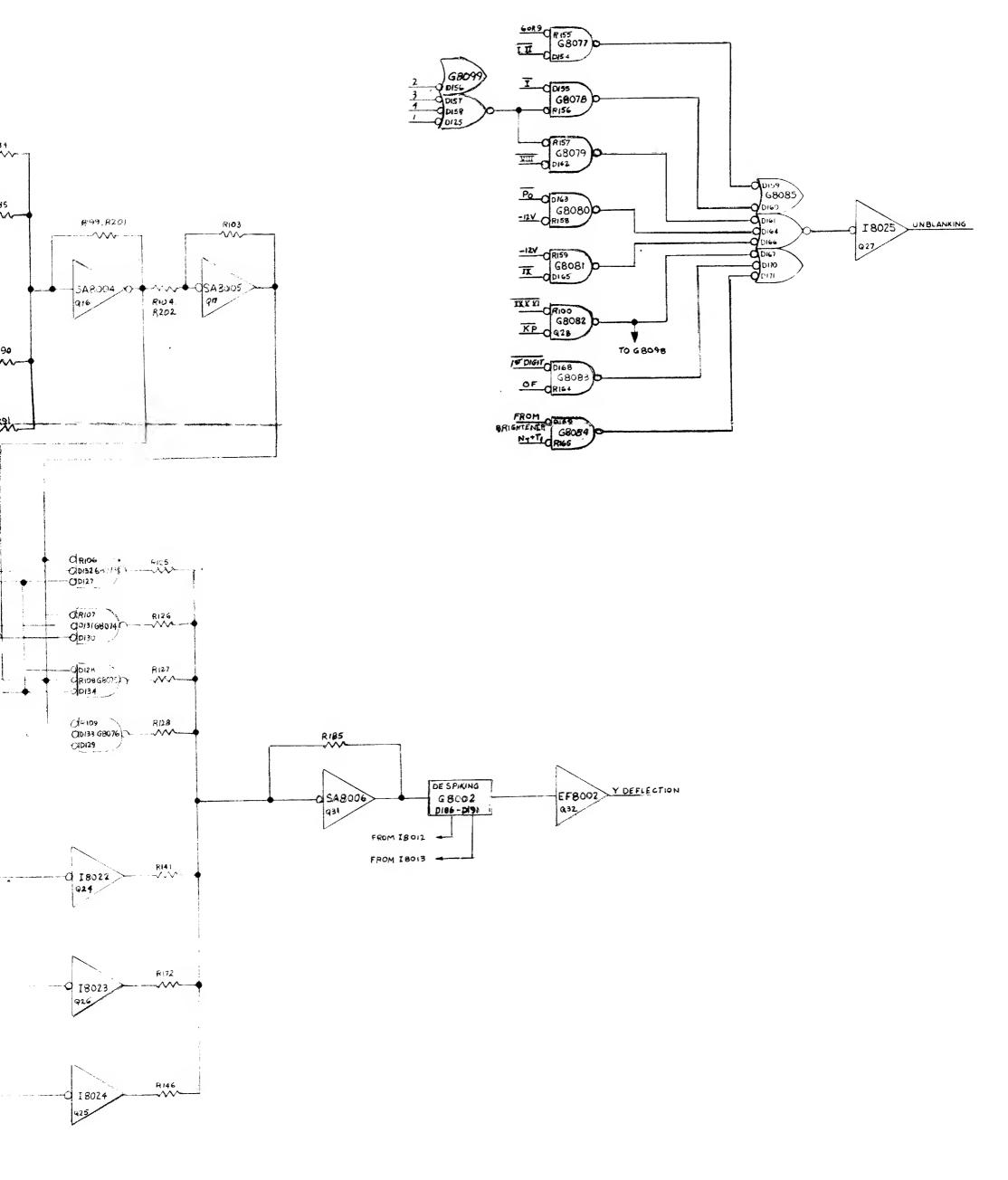


FIG. 6-34; OPTICAL CODER





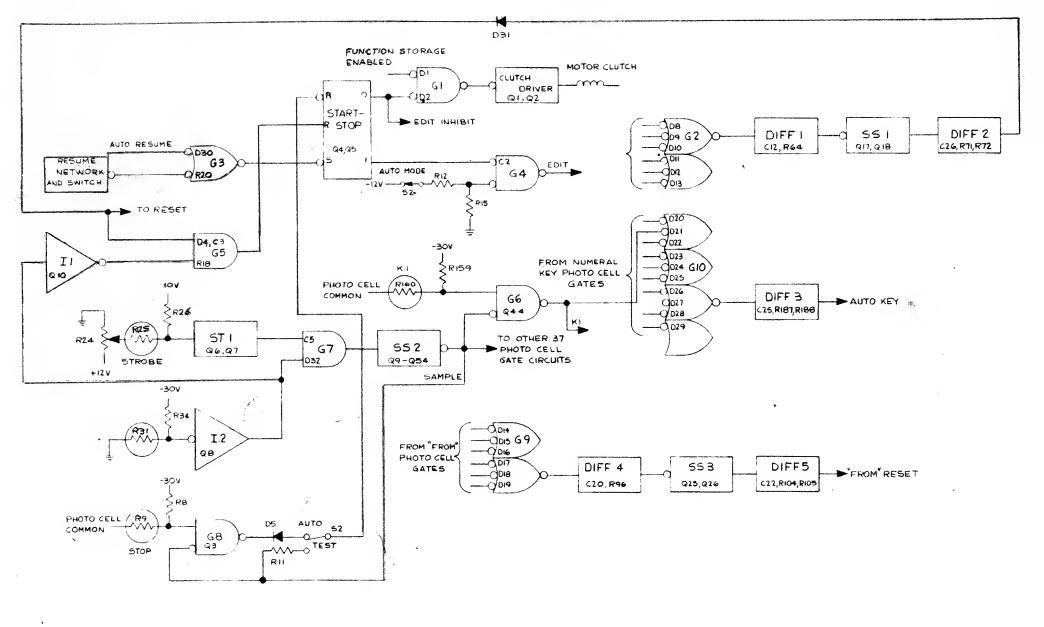


FIG. 6-35 CARD READER

